

REMARKS¹

In the outstanding Office Action, the Examiner rejected claims 1-15 under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 6,169,700 to Luo et al. ("Luo"). By this amendment, Applicants have amended claims 1, 3, 8, 11, 12, and 14. Claims 1-15 remain pending in this application.

Applicants respectfully traverse the rejection of claims 1-15 under 35 U.S.C. § 102(b). "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference ... [t]he identical invention must be shown in as complete detail as is contained in the ... claim." MPEP § 2131 8th Ed. (Rev. 4), October, 2005 (internal citations omitted). Luo cannot anticipate claims 1-15 because Luo fails to teach each and every element recited in claims 1-15, as amended.

For example, amended claim 1 recites a memory system including a "collision detect circuit [which] sets a collision flag ... the collision flag providing an indication that any of the at least two ports may have read or written corrupted data." Luo fails to teach at least this element. At page 4 of the Office Action, the Examiner appears to assert that same location signal SAME_LOC of Luo corresponds to Applicants' claimed "collision flag." To the extent that same location signal SAME_LOC can reasonably correspond to Applicants' claimed "collision flag," the same location signal SAME_LOC does not "provid[e] an indication that any of the at least two ports may have read or written corrupted data," as recited in amended claim 1.

Rather, Luo teaches:

¹ The Office Action contains a number of statements reflecting characterizations of the related art and the claims. Regardless of whether any such statement is identified herein, Applicants decline to automatically subscribe to any statement of characterization in the Office Action.

dual port memory 100 importantly includes an asynchronous, simultaneous access wait state generator module 110 to handle the particular situation when both address decoders 102, 104 happen to be accessing the memory element at precisely the same time. In such a case, a wait signal ... is generated by the asynchronous simultaneous wait state generator module 110 to cause one of the simultaneously, asynchronously accessing processors to halt clocking of its port, or wait, until release by the asynchronous wait state generator module 110 (col. 4, lines 30-40, emphasis added),

and

[t]he wait state generator 123 is activated by an activation of the same location SAME_LOC signal generated by the simultaneous access determination module 120 (col. 5, lines 55-57).

Luo thus teaches generating the same location signal SAME_LOC when more than one port is attempting to simultaneously access a memory element, the same location signal SAME_LOC in turn activating a wait state generator 110, *which merely causes one of the ports to stop and wait*.

Luo does not teach that SAME_LOC, or any other signal, “provid[es] an indication that any of the at least two ports may have read or written corrupted data,” as recited in amended claim 1.

Because Luo fails to teach each and every element recited in claim 1, Luo cannot anticipate claim 1. Accordingly, claim 1 is allowable over Luo, and claims 2-7 are allowable at least due to their dependence from claim 1.

Amended claims 8, 11, and 14, although of different scope, recite elements similar to those recited in claim 1. That is claims 8, 11, and 14 also recite combinations including “[a] collision flag providing an indication that [at least one port] may have read or written corrupted data,” and are allowable over Luo for at least the same reasons given above with respect to claim 1.

Moreover, claims 9 and 10 depend from claim 8, claims 12 and 13 depend from claim 11, and claim 15 depends from claim 15. Thus, claims 9 and 10, claims 12 and 13, and claim 15

respectively require all of the elements recited in claims 8, 11, and 14 and are allowable at least due to their respective dependence from claims 8, 11, and 14. Applicants therefore respectfully request that the Examiner withdraw the rejection of claims 1-15 under 35 U.S.C. § 102(b).

In view of the foregoing amendments and remarks, Applicants respectfully request reconsideration and reexamination of this application and the timely allowance of the pending claims.

Please grant any extensions of time required to enter this response and charge any additional required fees to our deposit account 06-0916.

Respectfully submitted,

FINNEGAN, HENDERSON, FARABOW,
GARRETT & DUNNER, L.L.P.

Dated: June 23, 2006

By: 

Gary J. Edwards
Reg. No. 41,008

EXPRESS MAIL LABEL NO. EV 860820282 US
